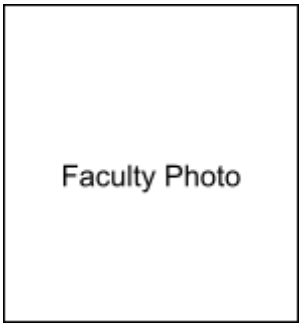
Faculty Profile: Dr. H V R ARADHYA



Brief Profile (Few Paragraphs)

Personal Information

- **Name:** Dr. H V RAVISH ARADHYA
- **Designation:** Professor and HOD
- **Department:** Electronics and Communication Engineering
- **Email:** ravisharadhya@rvce.edu.in, hod.ec@rvce.edu.in
- **Phone:** 68188178, 68188179
- ORCID: 0000-0003-3076-9120
- Researcher ID: 0-6994-2016
- Semantic Scholar ID: 0000-0002-8535-9789

Google Scholar / ResearchGate / LinkedIn: [Link if applicable]/ **ORCID: [Link]**
Google Citations: https://scholar.google.com/citations?hl=en&user=T0QNp0kAAAAJ
Scopus Citations:
http://www.scopus.com/authid/detail.url?authorId=55616592800
WOS Citations:
https://publons.com/researcher/2206552/ravish-aradhya-h-v/
Mendeley Citations:
https://www.mendeley.com/reference-manager/library/all-references
ORCID.ORG:
https://orcid.org/my-orcid?orcid=0000-0003-3076-9120
Semantic Scholar Citations:
https://www.semanticscholar.org/author/H.-V.-Ravish-Aradhya/19255649
Linkedin:
https://www.linkedin.com/in/dr-ravish-aradhya-h-v-57902bab/
RVCE website link:
https://rvce.edu.in/ec-ravisharadhya

Domain of Expertise

Research Focus

- **Primary Area:** VLSI Design and Verification
- **Allied Areas:**
  - Embedded Systems
  - Computer Architecture, VLSI forImage processing

Academic Qualifications

- **Ph.D.**: [VLSI Dseign], [Visvesvaraya Technological University], [2014]

  [Thesis Title: Design, Optimization and Synthesis of Low Power Reversible Logic ALU Components]

- **M.E**: [Electronics], [Bangalore University], [1995]
- **B.E**: [Electronics], [Bangalore University], [1991]

Professional Experience

Experience			
S.No	**Institute/College/Industry**	**Job Title**	**Duration (From- To)**
1.	RVCE, B'lore-560059	Professor & HOD	**Jul-2022-Till date**
2.	RVCE, B'lore-560059	Professor and Associate Dean	**Jun-2016-June-2022**
3.	RVCE, B'lore-560059	Associate Professor	Dec-2006 – Jun-2016
4.	RVCE, B'lore-560059	Assistant Professor	Oct-1997 – Nov-2006
5.	DSCE, B'lore	Lecturer	Jun 1996 – Oct 1997

Publications & Patents

	Details as on 21.05.2025	
Sl. No.	**Published by**	**Number**
1.	**International Journals**	**51**
2.	**International Conferences**	**85**
3.	**National Conferences**	**24**
4.	**PhD Forum**	**03**
	Total Number of Publications	**163**

Journal Publications

1. Ravish Aradhya H V, Arunkumar P C, Shrish Shrinath Vaidya, Sanket M Mantrashetti, Abhishek G Dastikopp, Kishan S Murthy, Prakash Pawar (IIIT, Dharwad, India), **"A Novel TriNet Architecture for Enhanced Analog IC Design Automation",** ***IEEE Transactions on Very Large Scale Integration Systems,*** Sep 2024. No. TVLSI-00159-2024.R2, Vol. 32, No. 11, Nov 2024, pp. 2046-2059,

(Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=10672521)
(Q1 Journal). (WOS, Sci and Scopus indexed)

2. H V Ravish Aradhya, Arunkumar P Chavan, S. M. Mantrashetti, P. Pawar, and O. S. Powar, **"A Novel Algorithm for Aspect Ratio Estimation in SRAM Design to Achieve High SNM, High Speed and Low Leakage Power",** in *IEEE Access*, vol. 13, pp. 9942-9954, 2025, DOI: 10.1109/ACCESS.2025.3527333.

(Download Link: https://ieeexplore.ieee.org/document/10833602)
(Q1 Journal). (WOS, Sci and Scopus indexed)

3. H V Ravish Aradhya, Wafa Naaz Shaik, Nandu Saseendran, **, "Digital Intellectual Property Verification using Universal Verification Methodology,"** International Journal of Creative Research Thoughts (IJCRT), Vol. 12, Issue. 06, June 2024, ISSN: 2320-2882, pp. C372-C377. (**UGC approved**).

(Download Link: https://ijcrt.org/papers/IJCRT2406258.pdf)

4. H V Ravish Aradhya, Neethu S, **"Evaluation of distributed denial of service attacks detection in software defined networks,"** IAES International Journal of Artificial Intelligence (IJ-AI), Vol. 13, No. 4, October 2024, pp. 4488~4498, ISSN: 2252-8938, DOI: 10.11591/ijai.v13.i4.pp4488-4498, **(Q2 Journal). (Scopus indexed).**

(Download Link: https://ijai.iaescore.com/index.php/IJAI/article/view/24988/14270)

5. H V Ravish Aradhya, Sushanth G**, "Hardware in Loop Network Simulators - An Insight Overview"** International Journal of Modeling, Simulation, and Scientific Computing, (**Q2 Journal**), Vol. 15, No. 01, ISSN (print): 1793-9623 | ISSN (online): 1793-9615, pp. 18305--18313 DOI: https://doi.org/10.1142/S1793962324300012, Feb 2023. World Scientific Publisher, **(Scopus and WOS Indexed)**. (Download Link: https://www.worldscientific.com/doi/abs/10.1142/S1793962324300012?journalCode=ijmssc)

6. H V Ravish Aradhya, Arunkumar P Chavan**, "Design of 5.1GHz Ultra-Low Power and Wide Tuning Range Hybrid Oscillator,"** International Journal of Electrical and Computer Engineering (IJECE), Vol. 13, No. 4, ISSN 2088-8708, e-ISSN 2722-2578, pp. 3778~3787, DOI: http://doi.org/10.11591/ijece.v13i4, Aug 2023. Institute of Advanced Engineering and Science (IAES), **(Scopus and WOS Indexed)**. (**Q2 Journal**), (Download Link: https://ijece.iaescore.com/index.php/IJECE/search/authors/view?firstName=Arunkumar&middleName=Pundalik&lastName=Chavan&affiliation=RV%20College%20of%20Engineering&country=IN)

7. Ravish Aradhya H. V, Ashish Kapania, **"Design Space Exploration of Power Efficient Cache Design Techniques,"** Advances in Networks and Communications, Book-1, ISBN: 978-3-642-17878-8_37, SPRINGER Berlin Heidelberg, Jan-2011, Vol. 132, pp. 362-371. DOI: 10.1007/978-3-642-17878-8_37. Part of the Communications in Computer and Information Science book series (CCIS, Volume 132)
(Download link: https://link.springer.com/chapter/10.1007/978-3-642-17878-8_37)

8. Mohana, Ravish Aradhya H V, **"Object Detection and Tracking using Deep Learning and Artificial Intelligence for Video Surveillance Applications,"** International Journal of Advanced Computer Science and Applications(IJACSA); West Yorkshire Vol. 10, Iss. 12, Jun 2019, pp. 517-530, e-ISSN: 2156-5570, p-ISSN: 2158-107X, Dec-2019. DOI:10.14569/IJACSA.2019.0101269 (**Scopus Indexed**).
(Download link: https://thesai.org/Downloads/Volume10No12/Paper_69-Object_Detection_and_Tracking_using_Deep_Learning.pdf) or https://www.ijitee.org/portfolio-item/H6362068819/)

9. Ravish Aradhya H. V, Shreyas H S, Arunkumar P Chavan, **"Design and Analysis of Low Power VCO Enabled Quantizer for CT Sigma Delta ADC,"** Indian Journal of Public Health Research & Development (IJPHRD), Vol. 10, Issue 5, Jun 2019, ISSN: 0976-0245, E-ISSN:0976-5506, pp. 921-927. DOI: 10.5958/0976-5506.2019.01197.5
(Download link: http://www.indianjournals.com/ijor.aspx?target=ijor:ijphrd&volume=10&issue=5&article=174)

Conference Papers:

1. Ravish Aradhya H. V. Gopal Kanase, Vinayakgouda Y G, **"RTL to GDSII of Harvard Structure RISC Processor"** 2021 IEEE International Conference on Electronics, Computing and Communication Technologies (**CONECCT-2021**), 978-1-6654-2849-1/21/$31.00 ©2021 IEEE, **DOI: 10.1109/CONECCT52877.2021.9622735**.

(Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9622735)

2. Ravish Aradhya H V, Arunkumar P C, Shrish Shrinath Vaidya, Sanket M Mantrashetti, Abhishek G Dastikopp, Kishan S Murthy, Prakash Pawar (IIIT, Dharwad, India), **"Integrating Neural Network Models for Advanced Automation in Analog Amplifier Circuit Design",** 2024 IEEE International Conference on Electronics, Computing and Communication Technologies (**CONECCT-2024**), Indian Institute of Science, 12-14 July 2024, Circuits, Devices & VLSI pp. 1-6, doi: 10.1109/CONECCT62155.2024.10677072.

(Download Link: https://ieeexplore.ieee.org/document/10677072)

3. H V Ravish Aradhya, Nethravathi K A, Rajath Duggal*, Samarth Patil, Rahul Anand Benni, **"Square Shape Microstrip Patch Antenna-Array With Defected Ground Structure: Versatile Design for Emerging 5G Communication Technologies and Beyond"** IEEE, 9 International Conference for Convergence in Technology (I2CT), 5-6, April 2024, The Fern-Hotel, Lonavala, Maharashtra 410401 (Rajath Duggal* - NOKIA India)
4. H.V. Ravish Aradhya, Neethu S, **"Approaches to providing Quality of Service (QoS) in Software-Defined Networking,"** International Conference on Technologies for Smart Green Connected Society 2021 (ICTSGS-1-2021) conference led by Yamagata University Japan, Nov, 29-30, 2021.
5. Ravish Aradhya H. V, Aravindkumar D. Gumtaj, Mohana, **"Real Time Smart, Intelligent and Novel Embedded Vehicle Interceptor for Security Applications,"** in the proceedings of 3rd SPRINGER - International Conference on "Emerging Research in Computing, Information, Communication and Applications (ERCICA-2015), 31st July – August 1st 2015 at NMIT Bangalore, India, pp-521-534. ISBN978-81-322-2553-9

(Download Link: https://link.springer.com/chapter/10.1007%2F978-81-322-2553-9_47)

6. Ravish Aradhya H V, Arun Kumar Chavan, Rohan A V, Pranshu Orian, Preetham Kaka **"Design and Implementation of Automated Industrial Robots in Cylinder Liner Production Lines,"** IEEE- 2021 Asian Conference on Innovation in Technology (ASIANCON), PCCOER, Pune, India, 28 - 29 Aug 2021. (WOS and Scopus Indexed-IEEE)

(Download Link: https://ieeexplore.ieee.org/document/9545017)

7. Ravish Aradhya H. V, Basaveswari Biradar, Robert Chan (Qualcom, USA), **"A Novel Technique to Optimize Regressions in L2 Cache Verification,"** in the proceedings of IEEE – 2nd International Conference on Inventive Research in Computing Applications (ICIRCA-2020), RVS College of Engineering and Technology, Coimbatore–641402, India, 15-17 July 2020. **pp. 1139-1142, ISBN:** 978-1-7281-5374-2/18/$31.00 © 2020 IEEE**.** (**Scopus indexed**)

(Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9183338)

8. Ravish Aradhya H. V and Karnati Gopi Manohar, **"Multiple Valued Logic (MVL) Based Combinational Building Blocks,"** in the proceedings of IEEE -International conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT-2016), Sri Venkateshwara College of Engineering, Bengaluru – 562 157, 20-21 May 2016. Pp: 2088-2092, [978-1-5090-0774-5/16/$31.00 © 2016 IEEE], **DOI: 10.1109/RTEICT.2016.7808207**. **(Scopus Indexed)**

(Download Link: http://ieeexplore.ieee.org/document/7808207/

9. Apoorva Raghunandan, Mohana Mohana, Pakala Raghav and H.V. Ravish Aradhya, **"Object Detection Algorithms for Video Surveillance Applications,"** in the proceedings of IEEE - 7th International Conference on Communication and Signal Processing (ICCSP 2018), 03-05 April 2018, Melmaruvathur, TN, India. 978-1-5386-3521-6/18/$31.00 ©2018 IEEE, PP. 563-568

   (Download Link: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8524461)

PhD Forum paper Presentations:

1. Mohana, Ravish Aradhya H. V, **"Design and Implementation of Object Detection, Tracking, Counting and Classification Algorithms using Artificial Intelligence for Automated Video Surveillance Applications,"** in Proceedings of ACCS 24th Annual International Conference on Advanced Computing and Communications (ADCOM 2018), pp. 119-122, 21-23 September 2018, at International Institute of Information Technology (IIIT-B), Organized by Advanced Computing and Communication Society (ACCS), Indian Institute of Science (IISc), Bangalore 560012, India, (PhD Forum paper Presentation), https://accsindia.org/adcom-2018-programme/, Published in ACCS open access digital library, https://journal.accsindia.org/.

2. Mohana, Ravish Aradhya H. V, **"Elegant and Efficient Algorithms for Real Time Implementation of Object Detection, Classification, Tracking and Counting using FPGA Zynq XC7Z020 for Automated Video Surveillance Applications,"** 10th IEEE Advanced Networks and Telecommunications Systems (ANTS-2016), 6-9 November 2016, J. N. Tata Auditorium, Indian Institute of Science (IISc), Bangalore, India.

3. Ravish Aradhya H V, Mohana, **"Design of Efficient Algorithms for Video Surveillance Applications using Artificial Intelligence,"** 25th IEEE Advanced Computing and Communications Conference (ADCOM 2019), 5-7 September 2019, at International Institute of Information Technology (IIIT-B), Bangalore, India.

Books/Book Chapters

One of the published books is the reference book at some of the leading universities; "***Basic Electronics,***" 1st Edition, McGraw-Hill (India) 2013, ISBN-13: 978-0-07-133310-8. (This book is in use as reference book at "The **University of Macau, Macau, China**" and "The **University of Mumbai**, Bombay, India, and "The **Manipal Institute of Technology**, Manipal, India."

1. Dr. Ravish Aradhya H. V., "Digital Integrated Circuits - *A Comprehensive Approach for System Design and Analysis*," 1st Edition, Oxford University Press (India) 2015, ISBN: (In progress-60% completed).
2. Dr. Ravish Aradhya H. V., "Linear ICs-A System Design Perspective," 1st Edition, Oxford University Press (India) 2015, ISBN: (In progress-30% completed).
3. Reviewed Gate-2014 material, Pearson Education (I) Pvt. Ltd., July-2014.
4. Ravish Aradhya H. V., "Basic Electronics," 1st Edition, McGraw-Hill (India) 2013, ISBN-13: 978-0-07-133310-8. (This book is in use as reference book at "The **University of Macau, Macau, China**" and "The **University of Mumbai**, Bombay, India, and "The **Manipal Institute of Technology**, Manipal, India."
5. Moris M. Mano, "Digital Design," 4th Edition, ISBN: 978-81-317-1450-8, Pearson Education (India), Adapted, 2007 (Adapted to Indian University requirements).
6. Moris M. Mano, "Digital Design," 4th Edition, ISBN: 978-81-317-0345-8, Pearson Education (India), Adapted, 2007 (Adapted to JNTUniversity requirements).
7. Moris M. Mano, "Digital Design," 4th Edition, ISBN: 978-81-317-0345-6, Pearson Education (India), Adapted, 2007 (Adapted to Anna University requirements).
8. Moris M. Mano, "Digital Design," 3rd Edition, ISBN: 978-81-317-0091-4, Pearson Education (India), Adapted, 2006 (Adapted to Indian University requirements).
9. Moris M. Mano, "Digital Design," 2rd Edition, ISBN: 978-81-780-8555-5, Pearson Education (India), Adapted, 2006 (Adapted to Indian University requirements).
10. L. Nashelsky and R. Boylestead, "Electronics Devices & circuits theory," 10th Edition, ISBN: 978-81-317-2700-3, Pearson Education (India), Adapted, 2009 (Adapted to Indian University requirements).
11. L. Nashelsky and R. Boylestead, "Electronics Devices & circuits theory," 9th Edition, ISBN: 978-81-775-8158-4, Pearson Education (India), Adapted, 2007 (Adapted to Indian University requirements).
12. Bhaskara -"Switching theory and logic design," ISBN: 978-12-590-0442-1, McGraw-Hill (India), Reviewed, July-2011.
13. Bhaskara -"VLSI design," ISBN: NA, McGraw-Hill (India), Reviewed, June-2011.

Patents [Filed / Published / Granted]

Tiny Tape-outs: [Patent Title].

1. RTL Design and Implementation of MAC unit using Dadda multiplier and Kogge-stone Adder submitted to tiny tapeout 8 in the year 2024
2. 2.RTL Design and Implementation of Dynamic Power Management unit submitted to tiny tapeout 8 in the year 2024

R & D Grants & Consultancy Projects

Ongoing & Completed Research Projects

- **[Project Title]** – Funding Agency: [Name], Duration: [Year-Year], Role: [PI/Co-PI].
- **[Project Title]** – Funding Agency: [Name], Duration: [Year-Year], Role: [PI/Co-PI].

Ongoing & Completed Consultancy Projects

- **[Training program for BEL Engineers/Scientists]** – Funding Agency: [BEL], Duration: [2018-Till date], Role: [Trainer].
- **[Software/Firmware Development for Bidirectional Data transfer between Cloud/SD Card and ARINC/CAN Bus]** – Funding Agency: [AutoTEC Systems Pvt Limited], Duration: [One Year], Role: [Co-PI].

Professional Memberships

- Life Member at ISTE (LMISTE_LM32215)
- Life Member at IETE (LMIETE-M133086)

Awards & Recognitions

- [BEST TEACHER AWARD], [Carrier Launcher (India), Bangalore], [May 2006]
- [BEST TEACHER AWARD], [ISTE-RVCE Chapter], [Sep 2016]

- [BEST RESEARCH PAPER AWARDS]
- Recipient of "Best Research Paper Award" from International Academy of Science, Engineering and Technology in International Journal of Electronics and Communication Engineering (IJECE), ISSN: 2278-991X, Dec-2014. IF-3.329, for the paper titled "Design and Optimization of Reversible carry look ahead Adder Circuit." (PhD research outcome).
- Recipient of "Best Research Paper Award" from IEEE-International Conference on Engineering and Technology (ICETECH-2015), Mar-2015. IF-3.329, for the paper titled "Design of square spiral Nano-antenna in infra-red region for Solar Energy Harvesting," conducted by Rathinam Institute of Technology, Coimbatore, Tamilnadu, India. IEEE Explorer: 978-1-4799-7678-2/15/$31.00, ©2015 IEEE, (Conference Record Number: #35961), 20th March 2015, pp:1026-1031.
- Recipient of "Best Research Paper Award" from IEEE-International Conference on 'Innovative Mechanisms for Industry Applications' (ICIMIA-2017), 21-23 Feb 2017, for the paper titled "Implementation of Highly Efficient Sorting Algorithm for Median Filtering using FPGA Spartan-6," conducted by Dayananda Sagar College of Engineering, Bengaluru, India. 978-1-5090-5960-7/17/$-31.00, ©2017 IEEE, ISBN: 978-1-5090-5959-1, (Conference Record Number: #35961), 21-23 Feb 2017, pp. 265-269.
- Recipient of "Appreciation Award" from Sri Venkateswara College of Engineering (SVCE, B'luru) for supporting (Session Chair) the conduction of IEEE International Conference on Recent Trends in Electronics Information and Communication Technology (RTEICT-2017) on 19-20 May-2017.

- Recipient of "Appreciation Award" from Sri Venkateswara College of Engineering (SVCE, B'luru) for supporting (Session Chair) the conduction of IEEE International Conference on Recent Trends in Electronics Information and Communication Technology (RTEICT-2016) on 20-21 May-2016.

Student Supervision

- **Ph.D. Candidates:** [06] (Graduated-02)
- **M.Tech Students:** [50]
- **Undergraduate Research Mentees:** [100]

Professional Roles

- **Editorial Board:** [Journal Name]
- **Chair/Committee Member:** [Conference Name, e.g., *IEEE International Conference on Robotics*]
- **Research Activities at International Level (With details):**

1. Review Committee member for Elsevier's Microelectronics Journal (MEJ).
2. Review Committee member for Springer's Journal of Computational Electronics (JCEL).
3. Review Committee member for Springer's Journal of Computational Electronics (JCEL).
4. Reviewed papers for IEEE International Conference on Recent Trends in Electronics, Information and Communication Technology (RTEICT-2016) on 20-21 May 2016 at Sri Venkateshwara College of Engineering, Bengaluru 562 157
5. Reviewed papers for IEEE-International Conference on Trends in Automation, Communication and Computing Technology (ITACT-2015) on 21-22 DEC 2015 at Acharya Institute of Technology and Management, Bengaluru 560 107.
6. Reviewed papers International Conference on Engineering, Science, Management and Advances in Research Technology & Engineering (ICESMART-2015) for on 29-30 Apr 2015 at T. Jhon Institute of Technology and Management, Bengaluru 560 083.
7. Reviewed papers for VLSISATA-2015 International conference at Amritanandamaye College of Engineering, Bengaluru.
8. Reviewed papers for VDAT-2015, 19th International Symposium on VLSI Design and Test, Bengaluru.

Teaching

Core Courses: [Current semester]

- [Course Code] [Name] (e.g., *Thermodynamics, Control Systems, VLSI Design*)
- [Course Code] [Name]
    - SystemVerilog for Design and Verification of Digital Systems
    - CAD Tools for VLSI design
    - Low Power VLSI Design,
    - System On Chip design
    - Digital System Design using VERILOG

- Advanced Microcontrollers and Interfacing

Advanced/Lab Courses:

- [SystemVerilog for Design and Verification]
- [Digital System Design using VERILOG]
- [Advanced Microcontrollers and Interfacing]

Professional Roles

Responsibilities

- **Academic:** [HOD, BOS and BOE Chairperson]
- **Administrative:** [VTU Edusat-Subject Expert-Computer Organization and Architecture, Grading Advisory.]

External Connect

- Domain expert (selection committee member) at UPSC_India, Recruitment panel member
- Domain expert (Departmental Promotion Committee-DPC member) at ISRO_India, panel member
- Corporate Trainer - Bharath Electronics Limited (BEL), C-DAC, Honeywell India, Manipal Academy of Higher Education (MAHE).
- Advisory board member-JSSATE, Bangalore.
- Advisory board member-Acharya ITM, Bangalore
- Principal Coordinator - 'VTU-EDUSAT,' an e-learning program; subject Expert for Computer Organization and Architecture
- Academic Co-chair- DVCON_India; Industry Conference
- BOS/BOE_Research-SBJ University, JSS University, Christ University.