Faculty Profile

Brief Profile

Personal Information

- **Name:** Dr. Shilpa D R
- **Designation:** Associate Professor
- **Department:** Electronics and Communication Engineering
- **Email:** shilpadr@rvce.edu.in
- **Phone:** 080-68188179

LinkedIn: www.linkedin.com/in/shilpadr/ **ORCID:** https://orcid.org/0000-0002-4292-7280

Domain of Expertise

Research Focus

- **Primary Area:** VLSI Design
- **Allied Areas:**
    - Digital System architecture –ASIC, SOC Design architecture
    - EDA tool development/frameworks

Academic Qualifications

- **Ph.D.**: [ECE], [VTU], [2017]
- **M.S**: [ASIC Design], [Mangalore University], [2010]
- **B.E.**: [ECE], [VTU], [2007]

Professional Experience

Experience

S.No	Institute	Job Title	Duration (From- To)
1.	R V College of Engineering	Associate Professor	2018-till date
2.	R V College of Engineering	Assistant Professor	2010-2018
3.	R V College of Engineering	Lecturer	2008-2010

Publications & Patents

Journal Publications

1. Nihar K.M, Sandesh Padiyar, Prajwal Bali, Shilpa D.R, Mahesh A , "Design of a source Degenated Cascode Stage Low Noise Amplifier for 5G Applications", *2022 ECS Transaction*, pp.107 2531.
2. Agarwal, Y., Shilpa, D.R.," Automotive Ethernet Physical Optimization and IEEE 1588 Implementation*", Lecture Notes in Electrical Engineering*, 2021, 748, pp. 489–500.
3. Nagesh, K.A., Shilpa, D.R," Verification of SerDes Design Using UVM Methodology", *Lecture Notes in Electrical Engineering*, 2021, 748, pp. 607–616
4. Shilpa D.R, Uma B.V, "Pascal Triangle based bus encoding for crosstalk optimization in SOC/ASIC", to be published in *International Journal of Advanced science and Technology*, May 2020.
5. Kumari Surbi, Shilpa D.R, " CPLD Interface Design for Board Design Applications", to be published in *International Journal of Advanced science and Technology*, May 2020.
6. Shilpa D R et.,Al, "IoT based Integrated Health Monitoring System", *International Journal of Engineering & Scientific Research(IJESR),* ISSN: 2347-6532,2018.

Conference Papers

1. S. D. R, V. R. Karjigi, H. M. Naik, V. Kumar and K. S. Marathe. Development of Automation Tool for Optimising Floorplan of a Given VLSI Design. *2022 IEEE 19th India Council International Conference (INDICON), Kochi, India.*2022; 1-6, doi: 10.1109/INDICON56171.2022.10039739
2. Raghunandan, A., Shilpa, D.R, "Design of Adiabatic Logic Circuits using FinFET 18nm Technology", *Proceedings 2nd International Conference on Communication, Computing and Industry 4.0,* C2I4 2021.
3. Shilpa, D.R., Rajith Kumar, B.K., Raghunandan, A., "Piezoelectric Energy Harvesting for Wearables" *Proceedings of 2nd International Conference on Communication, Computing and Industry 4.0*, C2I4 2021, 2021.
4. Apoorva R, Shilpa D.R, " Design of Electrostatic Energy Harvesting Pre charge Circuit", *in 4th International Conference on Communication and Electronics Systems (ICCES 2019),*in PPG Institute of Technology, Coimbatore, India from 17-19 July 2019.
5. Shreyas V Raj, Shilpa D.R, Revanasiddappa P.H, "Design and Implementation of FPGA based Pheripheral controllers for Computer Numeric Controller*", International Conference on Computer Science, Industrial Electronics (ICCSIE)* held at Mysuru, India on 26 June, 2019.
6. Shreyas V Raj, Shilpa D.R, Revanasiddappa," Design and implementation of based on FPGA peripheral controller for Computer Numeric Controller*"*,in *International Journal of Industrial Electronics and Electrical Engineering(IJIEEE)*, vol.7,Issue.9, october 2019.
7. A. Raghunandan and D. R. Shilpa, "Design of High-Speed Hybrid Full Adders using FinFET 18nm Technology," *2019 4th International Conference on Recent Trends on Electronics, Information, Communication & Technology (RTEICT)*, Bangalore, India, 2019, pp. 410-415, doi: 10.1109/RTEICT46194.2019.9016866.
8. Shilpa D.R, Uma B.V, "Architectural Level Crosstalk Minimization: A Tool", *in Science Direct-Elsivier Procedia Computer science*, vol.93, pp 117-121,2016.
9. Shilpa D.R, Uma B.V," Novel Zero Crosstalk Encoding/decoding techniques for SOC", in *2015 IEEE International Advance Computing Conference (IACC*), pp. 968-972,2015.

Books/Book Chapters

1. Rajith Kumar B.K, Dr. Shilpa D.R,Dr. Uma B.V," Detection of Blood related diseases using Deep Neural Nets", in IGI Global (Book chapter) in *"Handbook of Research on Deep Learning Innovations and Trends"*,pp1-15,2019.
2. Rajithkumar B K, Uma B V, Shilpa D.R," Precision Agricultural farming", book by LAP Lambert Academic Publishing, ISBN-13 : 978-6200481511, 2020

R & D Grants & Consultancy Projects

Ongoing & Completed Research Projects

- **[Electrostatic Energy harvesting for self-powered medical wearable devices.]** – Funding Agency: [VGST], Duration: [2019-2023], Role: [PI].
- **[Modelling, Simulation, Comparative performance Evaluation and Firmware implementation of Adapting Digital Beam Forming Techniques for optimized irregular sub array based active phased array radar]** – Funding Agency: [DRDO], Duration: [2021-2023], Role: [Co-PI].

Professional Memberships

- Senior member IEEE

Student Supervision

- **M.Tech:** 40
- **Undergraduate Research Mentees:** 80

Professional Roles

- **Chair/Committee Member:** [CSITSS- 2024- Convener, CSITSS- 2023- Publication Chair, CSITSS- 2022- Publication Chair]
- **Industry Advisor:** Sierra Edge AI

Teaching

Core Courses:

- [21EC32IA] [Digital VLSI Design]
- [EC365TDE] [Algorithms for VLSI Design Automation]

Advanced/Lab Courses:

- Analog Integrated Circuit Lab, Digital VLSI Design

Professional Roles

Responsibilities

- **Academic:** [Associate Dean Placement and Training]
- **Administrative:** [Nodal officer UGC Utsah, Outcome based education committee member, Compliance online /offline documentation committee member, BOE member , academic advisory committee member, Counsellor ,Skill lab coordinator 7th sem]

External Connect

- Member BoE –MVIT