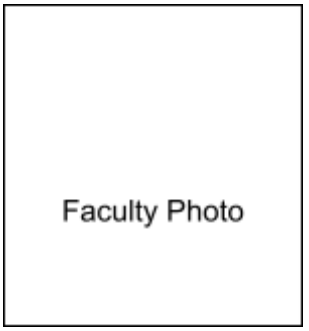
Faculty Profile



Personal Information

- **Name:** Dr. Sujatha Hiremath
- **Designation:** Assistant Professor
- **Department:** Electronics and Communication Engineering
- **Email:** sujathah@rvce.edu.in
- **Phone:** +91 9980471360

Google Scholar: https://scholar.google.co.in/citations?user=omZlZ6cAAAAJ&hl=en

ORCID: 0000-0003-4084-7372

Domain of Expertise: VLSI Design

Research Focus:

- **Primary Area:** Low Power VLSI design,
- Physical design
- VLSI testing

Academic Qualifications

- **Ph.D.**: Low Power VLSI design, VTU, 2023
- **M.Sc./M.Tech**: VLSI Design and Embedded Systems, VTU, 2009
- **B.E./B.Tech**: Electronics & Communication Engineering, Mangalore, 2001

Professional Experience

Experience			
S.No	**Institute/College/Industry**	**Job Title**	**Duration (From- To)**
1.	RVCE	Asst Professor Lecturer	2010 - Till date 2005- 2010

Publications

Journal Publications

1. Sujatha Hiremath, Sudeep Kumar B S, " Design and Analysis of Phase Locked Loop for SPI and I2C protocols", Journal of Harbin Engineering University ISSN: 1006-7043 Vol 45 No. 9 September 2024.

2. Sujatha S Hiremath, Huma Tabassum, and Krishna Prathik, "ADC Emulation on FPGA", INTL JOURNAL OF ELECTRONICS AND TELECOMMUNICATIONS, 2023, VOL. 69, NO. 3, PP. 425-430 July, 2023. DOI: 10.24425/ijet.2023.144379

3. Sujatha Hiremath, Vibha Narayan R, "Development of Verification Infrastructure to Validate RAM Low Power Features at Unit Level", International Journal of Engineering Research & Technology (IJERT), ISSN: 2278-0181 Vol. 11 Issue 07, July-2022.

4. Sujatha Hiremath, Sai Pranav G, "Physical Design Flow for Faster TAT in Lower Technology Nodes", International Journal of Engineering Research & Technology (IJERT), ISSN: 2278-0181, Vol. 11 Issue 06, June-2022.

5. Sujatha Hiremath, Dr Deepali Koppad, "ALU Design using Low Power Standard Cells", International Journal of Electrical Engineering and Technology (IJEET), Volume 11, Issue 6, August 2020, pp. 94-100.

6. Sujatha Hiremath, Natesh Gowda, "Layout Verification of Hard Macros", International Journal of Electrical Engineering and Technology (IJEET), Volume 11, Issue 4, June 2020, pp. 135-140.

7. Sujatha Hiremath, Rachana, "Link State Machine of PCI Express", International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 – 8958, Volume-9 Issue-4, April, 2020.

8. Sujatha Hiremath, Bhagyashree Atharga, Anurag Chandan, "Verification of Accessibility and Connectivity of Multi-Die Module Through TAP Interface, International Journal of Recent Technology and Engineering (IJRTE)', ISSN: 2277-3878 (Online), Volume-8 Issue-1, May 2019. Page No.:2077-2082.

9. Sujatha Hiremath, Dr. Deepali Koppada, " Low Power Multiplier and Divider circuit using GDI", International Jourals of Engineering & Applied Sciences, vol 12, Issue:12 page no: 9424-9429.2017, ISSN:1816-949X.

10. Sujatha Hiremath, Monish N K, " An Efficient Structure for SQRT Carry Select Adder with Reduced Delay and Area for High Speed Processing Applications", International Journal of Trend in Research and Development, Volume 4(6), page no 448-454, Nov-Dec-2017, ISSN: 2394-9333

11. Sujatha Hiremath, Dr. Deepali Koppada " Low Power VLSI circuits using Modified Gate Diffusion Input (GDI)", IOSR Journal of VLSI and Signal Processing (IOSR-JVSP), vol 4, Issue 5, ver II, (Sep-Oct 2014) pp 70-76.

12. Sujatha Hiremath and Naveen S M, “Design and Implementation of multiplier circuit for complex numbers”, International journal of Combined Research & Development (IJCRD) vol 2, issue 6, June 2014, pp 33-37.

13. Sujatha Hiremath & Raju Patil,” FPGA Implementation of Smart Multi Protocol Translator”, International Journal of Scientific & Engineering Research, Volume 4, Issue 7, July 2013

Conference Papers

1. Sujatha Hiremath, Udaykrishna, “ What if analysis of safety Mechanism’s impacts on ETHMAC design under Functional safety flow”, Design & Verification Conference and Exhibition DVCON-22, 5-6th September, Bengaluru, India

2. Sujatha Hiremath, Dr Deeplai Koppad, “ Design of Low Power Sequential Circuits using GDI Cells”, 3rd International Conference on Inventive Computation & Information Technologies (ICICIT) 2021, Springer, August 12-13, 2021

3. Sujatha Hiremath, Vinayakgouda, “ RTL to GDSII implementation of Advanced High-Performance Bus Lite”, 6th International Conference on Communication and Electronics Systems (ICCES 2021), 8-10 July 2021, Coimbatore, Tamil Nadu.

4. Sujatha Hiremath & Ranjitha H V, “Low Power Design and Implementation of Multi-Output Carry Look-Ahead Adder”, 3 rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT-2018), MAY 18th & 19th 2018.

5. Sujatha Hiremath & Divya P A “ A Novel Match-Line Sensing Technique for Low Power CAM array”, 3 rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT-2018), MAY 18th & 19th 2018.

6. Sujatha Hiremath & Ranjitha H V, “RTL Power Estimation: Early Design Cycle Approach for SoC Power Sign-Off”, 3 rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT-2018), MAY 18th & 19th 2018.

7. Sujatha Hiremath, Akshata Mathad, Amrutha Hosur, Dr. Deepali Koppad, “ Design of Low Power standard cells using Full Swing Gate Diffusion Input”, IEEE International conference on Smart Technologies for smart nation, REVA University ,Bengaluru. 17-19 August 2017

8. Sujatha Hiremath, Jayaprakash,” Design of Clock Duty Cycle”, IEEE International conference on Smart Technologies for smart nation, REVA University , Bengaluru. 17-19 August 2017.

9. Sujatha Hiremath and Dr. Deepali Koppad, “ 1-Bit Full Adder Circuit Using Modified Gate Diffusion Input (GDI)”, First IEEE International Conference on Micro and Nano Technologies, Modeling and Simulation, Malaysia, page no 65-68,March 2016.

10. Sujatha Hiremath and Archana S “Design and Implementation of Fiber Channel Data Analyser”, IEEE International Conference on International Conference on Control Computing Communication and Materials ICCCCM- 21st – 22nd Oct 2016

Books/Book Chapters

Control Systems, I K Publisher , ISBN 10: 9390620708 ISBN 13: 9789390620708
Publisher: IK international, 2021

Professional Memberships

- Membership: IETE Bangalore.

Student Supervision

- **M.Tech/M.Sc. Students:** [20]
- **Undergraduate Research Mentees:** [25]

Teaching

Core Courses: Physical Design, Low Power VLSI Design, ASIC Design, DFT, VLSI Testing, DSD usingVerilog HDL

- Advanced/Lab Courses: Low Power Digital IC Design Lab, Physical Design Lab

Responsibilities

- **Administrative:** PG Lab In-charge, NBA file incharge